REMARKS

Reconsideration of the application in view of the above amendments and the following remarks is requested. Claims 3, 5, 8-9, 12, 14, 17-20, and 23-36 are in this application. Claims 1-2, 4, 6-7, 10-11, 13, 15-16, and 21-22 have been cancelled. Claims 3, 5, 8, 14, 17-18, and 23-24 have been amended. Claims 25-36 have been added to alternately and additionally claim the present invention.

On August 28, 2002, applicant filed a paper entitled Request Permission To Make Drawing Changes, which was received by the PTO on September 03, 2002. The Request included red-line changes to FIGS. 4 and 6, adding reference label 250 to both figures. In Appendix A of the present paper, applicant attaches Replacement Sheets for FIGS. 4 and 6.

The Examiner objected to the Abstract because the Abstract includes the acronym "CMOS." The Abstract has been amended to define the acronym "CMOS."

The Examiner rejected claims 17-22 under 35 U.S.C. §112, second paragraph, because claim 17 recites a second adder cell without the essential interconnection. Applicant notes that claim 17 recited a second adder cell connected to the first adder cell. In addition, claim 18 recited a third adder cell connected to the second adder cell.

However, to further prosecution, claim 17 has been amended to recite that the second adder cell is connected to receive a signal from the output of the first carry out circuit of the first adder cell. In addition, claim 18 has been amended to recite that the third adder cell is connected to receive a signal from the output of the second carry out circuit of the second adder cell.

As a result, claims 17 and 18 are believed to satisfy the requirements of the second paragraph of section 112. In addition, since claims 19 and 20 depend directly and indirectly from claim 17, claims 19 and 20 are believed to satisfy the

requirements of the second paragraph of section 112 for the same reasons as claim 17. In addition, as noted above, claims 21-22 have been cancelled.

The Examiner rejected claims 1-2, 4, 6-16, and 23-24 under 35 U.S.C. §102(b) as being anticipated by Takahashi (U.S. Patent No. 5,875,124). As noted above, claims 1-2, 4, 6-7, 10-11, 13, and 15-16 have been cancelled. In addition, claims 8-9, 12, 14, and 23-24 now depend directly or indirectly from claim 3.

The Examiner also rejected claims 1-3, 5-12, 14-17, and 23-24 under 35 U.S.C. §102(b) as being anticipated by Hmida et al. (U.S. Patent No. 4,920,509). Claim 3 has been amended to be in independent form and to include an additional limitation. For the reasons set forth below, applicant respectfully traverses this rejection as applied to claim 3.

Claim 3 recites, in part,

> "a first logic gate having a first input that receives a first input signal, a second input that receives a second input signal, and a first output that generates a first logic signal, the first input signal, the second input signal, and the first logic signal each having a logic state, the first logic gate generating the first logic signal in response to the logic states of the first and second input signals, the first logic gate generating an inverted first input signal in response to the first input signal;
>
> "a first inverter circuit having a third input that receives a third input signal, a fourth input connected to receive the first logic signal, a first output that generates an inverted third signal, and a second output that generates an inverted first logic signal;
>
> "a first carry out circuit having a first control input connected to receive the first logic signal, a second control input connected to receive the inverted first logic signal, and an output, the carry out circuit including a first multiplexer that passes a first received signal to the output of the first carry out circuit when the first logic signal has a first logic state, and passes a second received signal to the output of the first carry out circuit when the first logic signal has a second logic state, the first received signal being the first input signal; and
>
> "a first sum circuit having a first control input connected to receive the first logic signal, a second control input connected to receive the inverted first logic signal, a first sum input connected to the third input signal, a second

sum input connected to the inverted third signal, and an output, the second sum input and the output of the first sum circuit not be directly connected together."

In rejecting the claims, the Examiner pointed to element 100 shown in FIG. 2 of Hmida as constituting the first logic gate required by the claims, and inverters 201/202 and 401/402 shown in FIG. 2 of Hmida as constituting the first inverter circuit required by the claims. In addition, the Examiner pointed to the circuit shown in FIG. 2 of Hmida that generates the RiS carry output signal as constituting the first carry out circuit required by the claims, and the circuit shown in FIG. 2 of Hmida that generates the Si signal as constituting the first sum circuit required by the claims.

The circuit that generates the Si signal, however, can not be read to the first sum circuit required by the claims. For example, if transistors 204 and 205 shown in FIG. 2 of Hmida are read to be first sum circuit, then the gate of transistor 204 can be read to be the first control input because the gate is connected to the output of element 100. In addition, the gate of transistor 205 can be read to be the second control input because the gate is connected to the inverted output of element 100.

The right-side common terminal point of transistors 204 and 205 shown in FIG. 2 of Hmida can also be read to be the first sum input if the carry in signal Ri-1S is read to be third input signal. Thus, if the Si output is read to be the output of the first sum circuit, then there is no structure which can be read to be the second sum input required by claim 3. The left-side common terminal point of transistors 204 and 205 shown in FIG. 2 of Hmida can not be read to be the second sum input because claim 3 requires that the second sum input and the output not be directly connected together.

The same Si output circuit is illustrated in FIGS. 3, 4, and 5 of Hmida. In addition, the circuit which outputs the Si+1 signal in FIG. 5 of Hmida shows the same output circuit. Thus, since the Hmida reference fails to show a structure which can be read to be the second sum input, claim 3 is not anticipated by the Hmida

reference. In addition, since claims 5, 8-9, 12, 14, 17, and 23-24 depend either directly or indirectly from 3, claims 5, 8-9, 12, 14, 17, and 23-24 are not anticipated by Hmida for the same reasons as claim 3. As noted above, claims 1-2, 6-7, 10-11, and 15-16 have been cancelled.

The Examiner further rejected claims 1-6, 8-13, 15, 17-19, and 23-24 under 35 U.S.C. §102(b) as being anticipated by Mazin et al. (U.S. Patent No. 4,866,658). For the reasons set forth below, applicant respectfully traverses this rejection as applied to claim 3.

In rejecting the claims, the Examiner pointed to the exclusive OR gate shown in FIGS. 1-2 of Mazin as constituting the first logic gate required by the claims. The exclusive OR gate shown in FIGS. 1-2 of Mazin includes a first input (A), a second input (B), and two outputs. In addition, the Examiner pointed to the circuitry that generates the inverted Cout or the Cout signal as constituting the first carry out circuit.

As noted above, claim 3 recites that the first carry out circuit includes a first multiplexer that passes a first received signal to the output of the first carry out circuit when the first logic signal has a first logic state. In addition, claim 3 also recites that the first received signal is the first input signal. Thus, the first carry out circuit must include a multiplexer that receives and passes the first input signal when the first logic signal has the first logic state.

The Mazin reference, however, fails to teach or suggest a carry out circuit that includes a multiplexer as required by claim 3. In FIG. 1, the first input (A) can not be read to be the first input signal passed by the multiplexer because, although input (A) is passed by the transmission gate within the XOR circuit, input (A) is not passed by the NMOS transistor of transmission gate T3, the PMOS transistor of transmission gate T4, or the NMOS transistor of transmission gate T5. The input (A) is also not passed by transistors P1 and N2, and is inverted by inverter 15. Thus,

there is no structure which can be read to be a multiplexer that passes the signal on the input (A).

The second input (B) can not be read to be the first input signal passed by the multiplexer because input (B) is not passed by the NMOS transistor of transmission gate T1 or the PMOS transistor of transmission gate T2. The input (B) is also not passed by transistors P2 and N1, and is inverted by inverter 23. Thus, there is no structure which can be read to be a multiplexer that passes the signal on the input (B). (Similar comments apply to FIG. 2 of Mazin.) As a result, there is no structure which can be read to be a multiplexer, and no input signal which can be read to be the first input signal required by claim 3.

Since there is no structure which can be read to be a multiplexer and no signal which can be read to be the first input signal, the circuit identified by the Examiner can not be read to be the first carry out circuit. Thus, since Mazin fails to teach a first carry out circuit, claim 3 is not anticipated by Mazin. In addition, since claims 5, 8-9, 12, 17-19, and 23-24 depend either directly or indirectly from 3, claims 5, 8-9, 12, 17-19, and 23-24 are not anticipated by Mazin for the same reasons as claim 3. As noted above, claims 1-2, 4, 6, 10-11, 13, and 15 have been cancelled.

The Examiner rejected claims 14 and 20-22 under 35 U.S.C. §103(a) as being unpatentable over Mazin. Claims 14 and 20 depend either directly or indirectly from claim 3. (Claims 21-22 have been cancelled.) Applicant, however, can find nothing in Mazin which teaches or suggests a first carry out circuit as required by claim 3 (since there is no structure which can be read to be the multiplexer and no signal which can be read to be the first input signal). As a result, claim 3 is patentable over Mazin. Thus, since claims 14 and 20 depend either directly or indirectly from claim 3, claims 14 and 20 are patentable over Mazin for the same reasons as claim 3.

The Examiner rejected claims 3, 5, and 17 under 35 U.S.C. §103(a) as being unpatentable over Takahashi in view of either Hmida or Mazin. As noted above, claim 3 requires that the first carry out circuit include a first multiplexer that passes the first input signal. With respect to Takahashi, the Examiner pointed to elements 12, 22, 30, 40/42, and 50 shown in FIGS. 1A, 2A, 5, 6, and 7, respectively, of Takahashi as constituting the first logic gate of claim 3.

In addition, the Examiner pointed to the circuits shown in FIGS. 5-7 of Takahashi which output the Cout signal as constituting the first carry out circuit required by the claims. (FIGS. 1B and 2B of Takahashi show the carry out circuits, but do not show a multiplexer that passes an input signal. FIGS. 5-7 of Takahashi show similar Cout circuits.)

With respect to FIG. 7 of Takahashi, applicant assumes that the Examiner is reading transmission gate 302 to be part of the multiplexer required by the first carry out circuit of claim 3. Transmission gate 302, however, can not be read to be part of the multiplexer because Takahashi teaches that transmission gate 302 passes an inverted input signal rather than the input signal.

Thus, although Takahashi teaches that input signal B is input to element 50, Takahashi also teaches in FIG. 7 that the input signal B is inverted by inverter INV301 before being input to transmission gate 302. (Similar comments apply to the circuits shown in FIGS. 5 and 6 of Takahashi.) As a result, since Takahashi fails to teach a multiplexer that passes the first input signal, claim 3 is patentable over Takahashi.

With respect to Hmida, the Examiner pointed to input signal Ai shown in FIGS. 2-5 as constituting the first input signal of claim 3. In FIG. 2 of Hmida, applicant assumes that the Examiner is reading (XOR) element 100 shown to be the first logic gate, and the transmission gate defined by transistors 304/305 to be part of the multiplexer required by the first carry out circuit. (FIGS. 3 and 4 show similar

transmission gate structures. FIG. 5 of Hmida requires that the signal be inverted before being input to the transmission gate similar to Takahashi.)

The Examiner then argued that one skilled in the art would have been motivated to incorporate the input signal structure of Hmida into the full adder circuit of Takahashi to form a full adder. As noted above, FIG. 7 of the Takahashi reference shows a full adder that has an input signal B which is input to (XOR) element 50, and an inverter INV301 that inverts the input signal B before it is input to transmission gate 302.

Thus, to incorporate the input signal structure of Hmida into Takahashi, the Examiner appears to argue that one skilled in the art would be motivated to eliminate inverter INV301 shown in FIG. 7 of Takahashi. With inverter INV301 gone, the input signal B shown in FIG. 7 of Takahashi would be input to XOR element 50, and to transmission gate 302 in the same manner as Hmida.

However, if inverter INV301 is removed, XOR element 50 shown in FIG. 7 of Takahashi will not operate as intended. Since the combination of the two references would prevent the full adder from working as intended, one skilled in the art would not be motivated to incorporate the input signal structure of Hmida into the Takahashi circuit.

Thus, since one skilled in the art would not be motivated to combine the Hmida and Takahashi references, claim 3 is patentable over Takahashi in view of Hmida. In addition, since claims 5 and 17 depend either directly or indirectly from 3, claims 5 and 17 are patentable over Takahashi in view of Hmida for the same reasons as claim 3.

With respect to Mazin, applicant can find nothing in Mazin which teaches that input signal A shown in FIG. 1 of Mazin is passed by any multiplexer or transmission gate (other than the transmission gate T1 which is a part of the XOR gate). As a result, input signal A can not be read to be the first input signal of claim 3. Since input signal A shown in FIG. 1 of Mazin can not be read to be the first input signal, it

is unclear how one would incorporate the input signal structure of Mazin into Takahashi to read on claim 3. Thus, claim 3 is patentable over Takahashi in view of Mazin. In addition, since claims 5 and 17 depend either directly or indirectly from 3, claims 5 and 17 are patentable over Takahashi in view of Mazin for the same reasons as claim 3.

New claim 25 recites:

> "an exclusive OR circuit having a first input, a second input, an exclusive OR output, and a signal output;
> "an output circuit having:
> "a first transmission gate having a first input, a first gate, a second gate, and a first output;
> "a second transmission gate having a second input, a third gate connected to the second gate, a fourth gate, and a second output connected to the first output;
> "a third transmission gate having a third input, a fifth gate connected to the fourth gate, a sixth gate, and a third output;
> "a fourth transmission gate having a fourth input, a seventh gate connected to the sixth gate, an eighth gate, and a fourth output connected to the third output; and
> "an inverter having an input connected to the third input of the third transmission gate, and an output connected to the fourth input of the fourth transmission gate."

With respect to Takahashi, FIG. 7 shows an exclusive OR gate 50 which can be read to be the exclusive OR gate of claim 25. Gate 50 has an XOR output and a signal output (the inverted B signal). Takahashi also shows a transmission gate 302 with an input connected to the signal output of gate 50 in FIG. 7, which can be read to be the first transmission gate required by claim 25.

In addition, transmission gate 306 shown in FIG. 7 of Takahashi can be read to be the second transmission gate required by claim 25, transmission gate 308 can be read to be the third transmission gate required by claim 25, and transmission gate 310 can be read to be the fourth transmission gate required by claim 25.

However, if transmission gates 308 and 310 are read to be the third and fourth transmission gates, then there is no structure which can be read to be the inverter required by claim 25. Inverter INV303 shown in FIG. 7 of Takahashi has the wrong orientation, and thus can not be read to be the inverter required by claim 25.

As a result, new claim 25 is not anticipated by Takahashi. In addition, since claims 26-36 depend either directly or indirectly from 25, claims 26-36 are not anticipated by Takahashi for the same reasons as claim 25.

With respect to Hmida, claim 25 recites four transmission gates. From what applicant can determine, there are no structures in FIGS. 2-5 of Hmida that can be read to be the four transmission gates required by claim 25. As a result, new claim 25 is not anticipated by Hmida. In addition, since claims 26-36 depend either directly or indirectly from 25, claims 26-36 are not anticipated by Hmida for the same reasons as claim 25.

With respect to Mazin, FIGS. 1-2 show only three transmission gates outside of the XOR gate. As a result, there is no apparent structure which can be read to be the fourth transmission gate that is required by claim 25. As a result, new claim 25 is not anticipated by Mazin. In addition, since claims 26-36 depend either directly or indirectly from 25, claims 26-36 are not anticipated by Mazin for the same reasons as claim 25.

Thus, for the foregoing reasons, it is submitted that all of the claims are in a condition for allowance. Therefore, the Examiner's early re-examination and reconsideration are requested.

Respectfully submitted,

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APPENDIX

Replacement Sheets for FIGS. 4 and 6.